IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR UNITED STATES PATENT

SOLID STATE RELAY AND METHOD OF OPERATING THE SAME

Inventors: Michael M. Kugelman
Steven C. Simshauser

Filed: _____

SOLID STATE RELAY AND METHOD OF OPERATING THE SAME

[0001] This application claims priority from U.S. Provisional Application Serial No. 60/460,050 filed April 4, 2003.

BACKGROUND OF THE INVENTION

[0002] The present invention is related to solid state AC power switching, in general, and more particular, to a solid state relay for switching AC power to a load with reduced electromagnetic interference (EMI) or noise, and a method of operating the same.

[0003] With the increased use of electronic/computerized control and instrumentation systems on-board aerospace vehicles, it has become increasingly important to minimize the electromagnetic interference (EMI) or noise that is generated when switching AC power to electrical loads. Such EMI may have an adverse effect on the avionics, especially when generated over the AC power lines. Back-to-back solid-state switches, like field effect transistors (FETs), for example, have been used in solid-state relays (SSRs) for AC power switching in a variety of applications. Heretofore, these applications attempt to control the solid-state switches or FETs of the SSR simultaneously at zero voltage across the FET switches and/or at zero current therethrough. Due to inaccuracies of timing, exact switching at zero voltage and/or zero current is not effected which causes EMI to be inherently generated by the AC power switching. These timing inaccuracies are exacerbated when the power frequency is varying or unknown.

[0004] What is needed then is a solid-state relay that overcomes the drawbacks of the current solid-state relays by permitting AC power switching with minimal generation of EMI. A solid-state relay that is not dependent on switching timing accuracy or constant or known power frequencies is highly desirable.

SUMMARY OF THE INVENTION

[0005] In accordance with one aspect of the present invention, a solid state relay coupleable to first and second phase busses of an AC power source for switching power from the first and second phase busses to a load comprises: first and second power semiconductor switches connected in a series circuit configuration and coupleable to the first and second phase busses for switching power from the first and second phase busses to

the load, each of the first and second power semiconductor switches controllably operative in conductive and non-conductive states; first and second power diodes coupled respectively across the first and second power semiconductor switches; and a control circuit for monitoring a polarity relationship of the first and second phase busses and controlling the first and second switches between conductive and non-conductive states based on the monitored polarity relationship.

[0006] In accordance with another aspect of the present invention, a method of operating a solid state relay coupled to first and second phase busses of an AC power source for switching power from the first and second phase busses to a load comprises the steps of: including in the solid state relay a series circuit configuration of first and second power semiconductor switches for coupling to the first and second phase busses, and first and second power diodes coupled respectively across the first and second power semiconductor switches; enabling the solid sate relay to supply power from the first and second phase busses to the load; disabling the solid state relay from supplying power from the first and second phase busses to the load; monitoring a polarity relationship of the first and second phase busses; upon the solid state relay being enabled, controlling the first and second switches sequentially to a conductive state based on the monitored polarity relationship; and upon the solid state relay being disabled, controlling the first and second switches sequentially to a non-conductive state based on the monitored polarity relationship.

BRIEF DESCRIPTION OF THE DRAWING

[0007] Figure 1 is a circuit schematic of a conceptual embodiment of the present invention.

[0008] Figures 2-5 depict different circuit configurations of the embodiment of Figure 1 for the purposes of describing an exemplary operation thereof.

[0009] Figures 6 and 7 are more detailed circuit schematics of the embodiment of Figure 1.

[0010] Figures 8A-8G depict time waveforms suitable for describing an exemplary operation of the circuits depicted in Figures 6 and 7.

DETAILED DESCRIPTION OF THE INVENTION

[0011] Figure 1 is a circuit diagram of a conceptual embodiment of the present invention. Referring to Figure 1, dual switches K1 and K2 are coupled in series with a load R_L across an AC power source. The switches K1 and K2 are representative of solid-state switches which may be electronically controlled as will become more evident from the description found herein below. In the present embodiment, the AC power source is generated across one phase Φ_A and neutral N which provides an RMS AC voltage of approximately 115 volts, for example. However, it is understood that the AC power source may be also generated across two phases of a three phase or multi-phase power source in which case the AC voltage may be on the order of 200 volts RMS or greater, for example. If applied to an airborne vehicle, the frequency of the AC power source may be around 400 Hertz, but may vary anywhere from 300 to 800 Hertz, for example. Actually, the present embodiment may operate at frequencies in the thousands of Hertz.

[0012] Also in the present embodiment, a power diode D1 is coupled in parallel across switch K1 in a configuration to block current when the Φ_A voltage potential is positive with respect to the N voltage potential and another power diode D2 is coupled in parallel across switch K2 in a configuration to block current when the Φ_A voltage potential is negative with respect to the N voltage potential. In the embodiment of Figure 1, a solid-state relay (SSR) comprises switches K1 and K2 and power diodes D1 and D2. Accordingly, the circuit embodiment of Figure 1 permits operation of switches K1 and K2 to conduct and block current through the load R_L from the AC power source with minimal generation of EMI by utilizing the parallel coupled power diodes D1 and D2.

[0013] Figures 1-5 depict different circuit configurations illustrating an operation of the present embodiment in accordance with the broad principles of the present invention. In the circuit configuration of Figure 1, it is presumed that the SSR is turned off or disabled, both switches K1 and K2 are not conducting and the diodes D1 and D2 are blocking current from passing through the load. In the circuit configuration of Figure 2, the SSR is enabled or turned on and as Φ_A becomes positive with respect to N, one of the switches K2, for example, is controlled to a closed or conducting state. However, in this state, diode D1 continues to block current through the load from Φ_A to N. In the circuit configuration of Figure 3, with the SSR enabled or turned on, as the voltage polarity of Φ_A changes from positive to negative with respect to N, current begins gradually to flow through the load via switch K2 which had been closed and conducting diode D1. In this state, the other of the

switches K1 is controlled to a closed or conducting state. Over the time period switch K1 is closing, load current gradually transitions from diode D1 to switch K1. In the circuit configuration of Figure 4, switch K1 finally closes. Thus, the parallel coupled diode D1 allows load current to flow initially until switch K1 is able to conduct the full load current as Φ_A changes from positive to negative with respect to N. Note that as K1 starts conducting, there is a smooth transition of the load current from D1 to K1. As a result, little or no EMI is generated during the switching of the AC power from off to on through the load.

[0014] Should the SSR be turned off in the circuit configuration of Figure 4, as Φ_A becomes positive with respect to N, one of the switches K2 is controlled open while the other switch K1 remains closed as shown in Figure 5, but load current continues to flow through the parallel coupled diode D2. That is, as switch K2 is opening, the load current gradually transitions from switch K2 to diode D2. Then, as Φ_A becomes negative with respect to N, diode D2 blocks the load current. While Φ_A is negative with respect to N , switch K1 may be opened without affecting current flow which is already blocked by diode D2. As a result, little or no EMI is generated during the switching of the AC power from on to off through the load. In addition, utilizing the parallel coupled diodes D1 and D2 eliminates substantially the critical zero crossing timing heretofore needed to switch the AC power on and off to the load. The parallel coupled diodes inherently commutate on and off to conduct and block load current as the respective switch is turned on and off at any frequency of the AC power source.

[0015] Figure 6 is a circuit schematic of a more detailed embodiment of the present invention. Referring to Figure 6, a floating DC power supply 10 is created between the voltages busses Φ_A and Φ_B of the AC power source. Phase Φ_B may be the neutral bus N or another phase of a multi-phase power source. In the present embodiment, the solid-state switches K1 and K2 as described in connection with Figure 1 are embodied by power N-type, metal oxide semiconductor (MOS) FETs FET-1 and FET-2, respectively, which may be of the type manufactured by Advanced Power Technology under the model no. APT5015, for example. Each APT 5015 package includes a power diode coupled across the FET anode-to-source (S) and cathode-to-drain (D). That is, diode D1 is coupled across FET-1 and diode D2 is coupled across FET-2. The switches FET-1 and FET-2 are coupled together in series at the source junctions thereof and together coupled across the busses Φ_A

and Φ_B in series with the load R_L 14 which in the present embodiment is a heater element, for example.

[0016] The floating power supply 10 comprises a resistor R1 having one end coupled to the Φ_B (phase B) power bus and the other end coupled to the anode of a diode D3. The cathode of diode D3 is coupled to the cathode of a zener diode D4 which may be a 12V zener, for example, and one side of a capacitor C1 which is coupled in parallel across the zener D4. The anode of D4 is coupled to the source junction of FET-1 and the anode of D1. The drain junction of FET-1 and cathode of D1 are coupled to the Φ_A (phase A) bus. Accordingly, each time the phase B bus goes positive with respect to the phase A bus, current is passed through the series connection of components R1, D3, D4, and D1 (half-wave rectification) and is limited by the resistance of R1 which for the present embodiment may be on the order of 20K ohms, for example, and the voltage developed thereacross. This current charges capacitor C1 which may be on the order of 10 microfarads, for example, to the voltage of the zener which may be 12 volts. Diodes D1 and D3 prevents C1 from discharging back to the phase B bus when it goes negative with respect to the phase A bus. The voltage across C1 is the voltage of the floating power supply 10. DC supply lines Vcc and Vss of the floating supply 10 are coupled to the positive and negative sides of C1, respectively.

[0017] Logic circuitry 12 for controlling the switching of switches FET-1 and FET-2 is coupled across the supply lines Vcc and Vss of the floating power supply 10. In the present embodiment, the collectors of separate photo-transistors PT1, PT2 and PT3 are coupled to the Vcc bus. The emitter of PT1 is coupled in series with a constant current sink diode D5 to the Vss bus and the emitter of PT2 is coupled in series with another constant current sink diode D6 to the Vss bus. The constant current sink diodes D5 and D6 may be of the type bearing model no. 1N5297, for example, and may conduct a predetermined current which may be on the order of 1 milliamp, for example. Each diode D5 and D6 acts as a switch which turns on to produce a substantially sharp rising edge voltage across the diode as the conduction current reaches the predetermined level. Prior to the conduction current reaching the predetermined level, the voltage across each diode D5 and D6 remains at substantially zero. Corresponding photodiodes PD1 and PD2 are coupled in parallel with each other and the parallel combination is coupled in series with a current limiting resistor R5 across the phase A and phase B busses. The photodiodes PD1 and PD2 may be embedded with their corresponding photo-transistors PT1 and PT2 in a common dual

optocoupler package which may be of the type manufactured by Fairchild under the model MCT 62, for example.

[0018] During the half-wave cycles of the AC power supply in which the phase A bus is positive with respect to the phase B bus, current passes through PD1 which produces light denoted as "POS" in response thereto. The POS light signal is optically coupled to the corresponding transistor PT1 to cause PT1 to conduct current through the diode D5. Likewise, during the half-wave cycles of the AC power supply in which the phase A bus is negative with respect to the phase B bus, current passes through PD2 which produces light denoted as "NEG" in response thereto. The NEG light signal is optically coupled to the corresponding transistor PT2 to cause PT2 to conduct current through the diode D6.

[0019] Referring to Figure 7, a photodiode PD3 corresponding to PT3 may be coupled in series with a switch S1 and a current limiting resistor R6 between a voltage source V+ and ground. The switch S1 may be a solid-state switch or an electromechanical switch operated by a controller, like a temperature controller, for example, for turning the SSR on and off to control temperature via the heater element. Switch S1 may be also a manually operated mechanical switch just as well. When switch S1 is operated to a conducting state, current passes through PD3 and PD3 generates light denoted as "ON" in response thereto. The PD3 and corresponding PT3 may be also packaged in a common opto-coupler component, like an MCT 62, for example. Referring back to Figure 6, the emitter of PT3 is coupled in series with a resistor R2 to the Vss bus. Accordingly, the light "ON" is optically coupled to PT3 and causes PT3 to conduct current from bus Vcc through resistor R2 to the bus Vss thus causing a positive voltage to be developed across resistor R2 with respect to Vss. In this manner, the logic 12 powered by the floating power supply 10 is totally isolated from the source of the control signals POS, NEG and ON via the optical coupling thereof.

[0020] Also, in the embodiment of Figure 6, the anode of D5 is coupled to a clock input denoted as CLK of a D-type flip-flop FF1 and the connecting node between the emitter of PT3 and resistor R2 is coupled to a data input denoted as D of FF1. An output Q1 of FF1 is coupled to the gate junction of FET-2 through a resistor R3 and coupled to a D input of another D-type flip-flop FF2. Further, the anode of D6 is coupled to a CLK input of FF2 and an output Q2 of FF2 is coupled to the gate junction of FET-1 through a resistor R4. Each flip-flop FF1 and FF2 is powered by the floating power supply via busses Vcc and Vss and operates to transfer the status of the signal at the D input thereof to the output Q at

the occurrence of a leading edge pulse at the CLK input and thereafter maintains the output Q until the next occurrence of a leading edge pulse at the CLK input.

[0021] An operation of the embodiment described in connection with Figures 6 and 7 will now be described utilizing the exemplary time waveforms of Figures 8A-8G. In operation, the switches FET-1 and FET-2 of the SSR are controlled by the logic circuitry 12 to switch the AC power supply (see Figure 8A) to the load or heater element 14. To achieve this objective, the opto-coupler PD1/PT1 causes a pulse denoted as POS at the CLK input of FF1 during the times when the phase A bus is positive with respect to the phase B bus as shown in Figures 8A and 8B. Likewise, the opto-coupler PD2/PT2 causes a pulse denoted as NEG at the CLK input of FF2 during the times when the phase A bus is negative with respect to the phase B bus as shown in Figures 8A and 8C. Note that until the SSR is enabled, the outputs Q1 and Q2 of the flip-flops FF1 and FF2 will remain in a low or non-positive state in response to the POS and NEG pulses. In these Q1 and Q2 states, switches FET-1 and FET-2 will remain open or non-conducting.

[0022] The SSR may be enabled to couple the AC power supply to the load via control of switches FET-1 and FET-2 by closing switch S1 which controls the opto-coupler PD3/PT3 to create a high or positive pulse denoted as ON at the D input of FF1. As shown in Figure 8D, pulse ON will remain in effect until switch S1 is opened. After enabling the SSR and at the leading edge of the next POS pulse, representative of a positive half-wave of the phase A bus, the FF1 generates a high or positive state at Q1 as shown by Figure 8E. The positive state at Q1 drives the switch FET-2 to begin closing and is provided to the D input of FF2. It may take a duration of time t1 within the positive half-wave cycle of the phase A bus for FET-2 to become fully conducting. In the present embodiment, time t1 may be approximately 300 microseconds, for example. Note that this closure of FET-2 will prepare for, but not permit current to be conducted to the load 14 since FET-1 remains open and diode D1 is in a blocking state.

[0023] However, as soon as the phase A bus becomes negative with respect to the phase B bus, diode D1 starts conducting current to the load 14 via previously closed switch FET-2 as shown in Figure 8G. At the leading edge of the next NEG pulse, representative of a negative half-wave of the phase A bus, the FF2 generates a high or positive state at Q2 (since D input is in a positive state) as shown by Figure 8F. The positive state at Q2 drives the switch FET-1 to begin closing. It may take a duration of time t2 within the negative half-wave cycle of the phase A bus for FET-2 to become fully conducting. In the present

embodiment, time t2 may be approximately 300 microseconds, for example. As FET-1 closes, load current gradually transitions from D1 to FET-1. Thus, when FET-1 is fully closed at the end of t2, it is conducting all of the load current.

[0024] The SSR may be disabled to decouple the AC power supply from the load via control of switches FET-1 and FET-2 by opening switch S1 which controls the opto-coupler PD3/PT3 to drop the ON pulse at the D input of FF1 as shown in Figure 8D. The pulse ON will remain low thereafter until switch S1 is closed again. At the leading edge of the next POS pulse, after disabling the SSR, the FF1 generates a low or non-positive state at Q1 as shown by Figures 8B and 8E. The low state at Q1 drives the switch FET-2 to begin opening and is provided to the D input of FF2. It may take a duration of time for FET-2 to become fully open or non-conducting. Note that this opening of FET-2 will prepare for, but not block current being conducted to the load 14 (see Figure 8G) since FET-1 remains closed and load current transitions to diode D2 which is in a conducting state. However, as soon as the phase A bus becomes negative with respect to the phase B bus, diode D2 becomes non-conducting. With D2 non-conducting and FET-2 open, current to the load 14 is blocked as shown in Figure 8G. Also, as the phase A bus becomes negative, the NEG pulse is generated (see Figure 8C) which triggers the output Q2 of the FF2 to a low or non-positive state which drives FET-1 to an open or blocking state.

[0025] Note that the SSR of the present invention creates no sharp load current transitions in switching the power supply to and from the load 14. Thus, the SSR is operational with little or substantially no EMI generation due to switching. Also, since the SSR of the present invention is not sensitive to zero switching timing, it may operate at varying frequencies of the AC power supply. Further, while the present SSR embodiment is described as controlling AC power to a resistive load, it is understood that it may also control AC power to loads other than resistive loads with minor modifications which are well within those persons of ordinary skill in the pertinent art. Still further, while the solid-state switches were embodied with MOSFETs in the present example, it is understood that other types of solid-state switches may be used, such as power bipolar transistors, insulated gate bipolar transistors (IGBTs) and the like, for example, without deviating from the broad principles of the present invention. Accordingly, the present invention should not be limited to any single embodiment, but rather construed in breadth and broad scope in accordance with the recitation of the appended claims.